The presently pending claims are original claims 1-19, of which claims 1 and 12 have been amended hereby, and new claims 23-26. Claims 1,12 and 23 are independent claims.

THE PRESENT INVENTION

The present invention provides an apparatus and method for enabling an interrupt under certain hardware conditions even though the interrupt has been masked by software. According to the teachings of the present invention, such an apparatus includes structure for indicating a software condition; structure for indicating a hardware condition; and structure responsive to both of the aforementioned structures for generating an interrupt in response to the assertion of an interrupt request signal.

THE CITED AND APPLIED ART

In the outstanding Official Action the Examiner cites and applies U.S. Patent 4,344,133 to Bruce, Jr. et al. This reference is directed to a method for synchronizing hardware and software. Bruce, Jr. et al. teach the providing of such synchronization by stopping the processor and setting a latch. If a non-masked interrupt then occurs, the latch is reset, preselected programmable registers of the processor can be stacked and an interrupt address is vectored to. If, on the other hand, a masked interrupt then occurs, the latch gets reset and the processor simply continues with the sequencing of instructions without servicing the interrupt. Bruce, Jr. et al. does not teach a system for disabling or overriding a masked interrupt under certain special conditions when such disabling or overriding would be extremely useful, even to the point of being essential for continued operation.

REGARDING THE TITLE

In the Outstanding Official Action the Examiner imposed a requirement for a title more clearly indicative of the invention to which the claims are directed. Applicants have endeavored to respond to the Examiner's requirement by the present amendment. The new title clearly indicates that the present invention is incorporated in processor or the like wherein interrupts may be masked and the new title also clearly indicates that the present invention is directed to interrupt mask disabling mechanisms and schemes.

REGARDING THE DRAWINGS

In the Outstanding Official Action the Examiner objected to FIG. 5 of the drawings because the drawings themselves do not include an indication that FIG. 5a and FIG. 5b together form FIG. 5. Applicants submit that they have overcome this objection by including such indication in the proposed substitute set of drawings submitted herewith. Approval of the proposed substitute sheet of drawings and withdrawal of the objection to FIG. 5 of the drawings are respectfully requested.

REGARDING THE SPECIFICATION

Applicants have amended the specification so that it now provides serial numbers and current status of all co-pending U.S. patent applications disclosed on pages 1-2 thereof.

REGARDING THE REJECTION OF CLAIMS 1-22

UNDER 35 U.S.C. §112, SECOND PARAGRAPH

In the outstanding Official Action the Examiner rejected claims 1-22 under 35 U.S.C. §112, second paragraph for allegedly being indefinite. In making this rejection the Examiner stated:

"As per claim 1, it is unclear if both the "software condition" and "hardware condition" are required to generate a single interrupt. Clarification and/or rephrasing is required.

As per claims 2-11, these claims incorporate the deficiencies of the parent claim.

As per claim 12, it is unclear if both the "software condition" and hardware condition" are required to generate a single interrupt. Clarification and/or rephrasing is required.

As per claims 13-22, these claims incorporate the deficiencies of the parent claim."

The rejection of claims 1-22 under 35 U.S.C. §112, second paragraph, is respectfully traversed. Applicants submit that the claims are worded in such a way that it is quite clear that both software and hardware conditions are considered in embodiments of the present invention. The use of the word "and" in the phrase "responsive to said indicated software condition and said indicated hardware condition" in claim 1 and similar phrases in other claims makes this clear. Also, the fact that both hardware and software conditions are mentioned in the various independent claims makes it clear that they are both considered. However, in certain embodiments of the present invention, only one condition or the other can trigger a final result. See, for example, new claim 26. This fact does not overcome the fact that the other condition was considered.

Based upon the foregoing, Applicants submit that the rejection of claims 1-22 under 35 U.S.C. §112, second paragraph, is without merit and withdrawal thereof in order.

REGARDING THE REJECTION OF CLAIMS 1-5 AND

12-16 UNDER 35 U.S.C. §102(b)

In the outstanding Official Action the Examiner rejected claims 1-5 and 12-16 under 35 U.S.C. §102(b) for allegedly being anticipated by Bruce, Jr. et al. In support of this rejection the Examiner said:

> As per claim 1, Bruce, Jr. et al. teach the claimed:
> "means for indicating a software condition; means for indicating a hardware condition": Bruce's means for indicating a software condition; means for indicating a hardware condition (see col. 1, lines 49-52); and
> "means for generating said interrupt in response to the assertion of said interrupt request line ..." (lines 6-9): Bruce's means for generating the interrupt in response to the assertion of the interrupt request line ... (see col. 8, lines 46-54).
> As per claim 2, Bruce teaches the "means for generating said interrupt" in col. 7, lines 63-65.
> As per claim 3, Bruce teaches the "means for enabling" and "means for asserting" in col. 8, lines 51-56.
> As per claim 4, Bruce teaches the "programmable register that outputs a software enable signal" in col. 1, lines 62-64.
> As per claim 5, Bruce teaches the "means for indicating said hardware condition comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal" in col. 2, lines 52-53.
> As per claims 12-16, these claims recite methods which parallel apparatus claims 1-5. In teaching the construction and use of the device, the reference of Bruce, Jr. et al. inherently teaches corresponding methods.

The rejection of claims 1-5 and 12-16 under 35 U.S.C. §102(b) for the reasons discussed above is respectfully traversed. As discussed hereinabove, Bruce, Jr. et al. teach synchronizing hardware and software; this is wholly different than overriding a masked interrupt. In fact, Bruce Jr. et al. specifically teach handling masked and unmasked interrupts conventionally.

Applicants, on the other hand, provide an unconventional method for handling masked interrupts only.

Based upon the foregoing, Applicants submit that Bruce, Jr. et al. neither disclose nor suggest the present invention as clearly claimed (i.e., the generating of an interrupt under special circumstances when it might not otherwise occur as desired is clearly set forth in the claims). Accordingly, Applicants further submit that the pending art rejection of claims 1-5 and 12-16 is without merit and withdrawal thereof in order.

SUMMARY AND CONCLUSION

In view of the fact that none of the art of record (including the cited but not applied art, all of which art has been carefully considered by the Applicants) discloses or suggests the present invention, as now defined by the independent claims, and in further view of the above amendments and remarks, reconsideration of the action and allowance of the present invention are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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